EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	30	(pla$2 or GLA$2 or PLD$2 or FPGA$2) same ((programmable near (logic device)) same (configurable with interface))	USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/14 22:11
L3	16	(712/1 712/32) and (pla$2 or GLA$2 or PLD$2 or FPGA$2) and ((programmable near (logic device)) and (configurable with interface))	USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/14 22:12
S1	19620	microcontroller	USPAT	OR	OFF	2004/08/03 10:37
S2	998	microcontroller and mux	USPAT	OR	OFF	2003/09/26 17:02
S3	0	microcontroller and mux and internal and external and peripharals	USPAT	OR	OFF	2003/09/26 17:03
S4	355	microcontroller and mux and internal and external and peripheral	USPAT	OR	OFF	2003/09/26 17:10
S5	0	(microcontroller and mux and internal and external and peripharals) and structurable	USPAT	OR	OFF	2003/09/26 17:05
S6	0	(microcontroller and mux and internal and external and peripharals) and structural	USPAT	OR	OFF	2003/09/26 17:04
S7	0	(microcontroller and mux and internal and external and peripharals) and intelligent and interface	USPAT	OR	OFF	2003/09/26 17:05
S8	83	(microcontroller and mux and internal and external and peripheral) and intelligent and interface	USPAT	OR	OFF	2004/08/03 10:41
S9	83	(microcontroller and mux and internal and external and peripheral) and intelligent and interface	USPAT	OR	OFF	2003/09/26 17:05
S10	0	(microcontroller and mux and internal and external and peripheral) and structurable	USPAT	OR	OFF	2003/09/26 17:05
S11	0	(microcontroller and mux and internal and external and peripheral) and "intelligent core" and interface	USPAT	OR	OFF	2003/09/26 17:06
S12	44	(microcontroller and mux and internal and external and peripheral) and intelligent and interface and core	USPAT	OR	OFF	2003/09/26 17:06
S13	10	(microcontroller and mux and internal and external and peripheral) and intelligent and interface and core and (process near data)	USPAT	OR	OFF	2003/09/26 17:07

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S14	7	((microcontroller and mux and internal and external and peripheral) and intelligent and interface and core and (process near data)) and circuit and dispose$1	USPAT	OR	OFF	2004/08/02 19:43
S15	7	((microcontroller and mux and internal and external and peripheral) and intelligent and interface and core and (process near data)) and circuit and dispose$1 and multiplexer	USPAT	OR	OFF	2003/09/26 17:09
S16	0	((microcontroller and mux and internal and external and peripheral) and intelligent and interface and core and (process near data)) and circuit and dispose$1 and multiplexer and configuration	USPAT	OR	OFF	2003/09/26 17:09
S17	165	microcontroller and internal and external and peripheral and circuit and dispose$1 and multiplexer and configuration	USPAT	OR	OFF	2003/09/26 17:11
S18	55	microcontroller and internal and external and peripheral and circuit and dispose$1 and multiplexer and configuration and array and NAND	USPAT	OR	OFF	2003/10/09 17:50
S19	1	microcontroller and DNF	USPAT	OR	OFF	2003/09/26 17:12
S20	46	microcontroller and internal and external and peripheral and circuit and dispose$1 and multiplexer and configuration and array and NAND and (state near machine)	USPAT	OR	OFF	2003/10/08 18:29
S21	11	microcontroller and internal and external and peripheral and circuit and dispose$1 and multiplexer and configuration and array and NAND and (state near machine) and fuse	USPAT	OR	OFF	2003/09/26 17:19
S22	9	microcontroller and internal and external and peripheral and circuit and dispose$1 and multiplexer and configuration and array and NAND and (state near machine) and fuse and reverse	USPAT	OR	OFF	2004/08/02 19:44
S23	108	("712"/ ".*") and program-controlled	USPAT	OR	OFF	2003/10/08 18:49
S24	2	("712"/ ".*") and program-controlled and (process near instruction$1)	USPAT	OR	OFF	2003/10/08 18:50
S25	1	("712"/ ".*") and program-controlled and (process near instruction$1) and internal and peripheral	USPAT	OR	OFF	2003/10/08 18:51
S26	11	("712"/ ".*") and program-controlled and intelligent	USPAT	OR	OFF	2004/08/02 19:42

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S27	1	("712"/ ".*") and program-controlled and intelligent and peripheral	USPAT	OR	OFF	2003/10/08 18:52
S28	2	("712"/ ".*") and program-controlled and intelligent and circuit and dispose$1 and multiplexer and configuration	USPAT	OR	OFF	2003/10/08 18:55
S29	2	("712"/ ".*") and program-controlled and intelligent and circuit and dispose$1 and multiplexer and configuration	USPAT	OR	OFF	2003/10/08 18:55
S30	2	"20020013630".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2003/10/09 17:53
S31	56447	"712"/ ".*"	USPAT	OR	OFF	2003/10/14 14:18
S32	37	("712"/ ".*") and fuse and "anti-fuse"	USPAT	OR	OFF	2003/10/14 14:19
S33	3	"6421754"	USPAT	OR	OFF	2004/08/02 20:04
S34	7	("5034907"|"5600845"|"5737235"|"5946219"|"6046603"|"6077315"|"6553395").PN.	USPAT	OR	OFF	2004/08/02 20:18
S35	7	("5848415"|"6029143"|"6134582"|"6212550"|"6292795"|"6330589"|"6563919").PN.	USPAT	OR	OFF	2004/08/02 20:18
S36	2459	(microcontroller microprocessor).ti.	USPAT	OR	OFF	2004/08/03 10:40
S37	0	(microcontroller microprocessor).ti. and @ad<="06061999"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 10:42
S38	120	(microcontroller microprocessor).ti. and @ad<="19990606" and (program$controll$2 program adj controll$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 13:19
S39	1	(microcontroller microprocessor).ti. and @ad<="19990606" and (program$controll$2 program adj controll$2) and peripheral$1 and unit$1 and memory and external and internal and intelligent and core and clock	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 10:46

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S40	0	(microcontroller microprocessor).ti. and @ad<="19990606" and (program$controll$2 program adj controll$2) and peripheral$1 and unit$1 and memory and external and internal and intelligent and core and clock and connection$1 and path$1 and strcuturable	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 10:53
S41	0	(microcontroller microprocessor).ab. and @ad<="19990606" and (program$controll$2 program adj controll$2) and peripheral$1 and unit$1 and memory and external and internal and intelligent and core and clock and connection$1 and path$1 and strcuturable	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 10:52
S42	0	(microcontroller microprocessor).ab. and @ad<="19990606" and strcuturable with hardware with unit$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 10:52
S43	0	strcuturable with hardware with unit$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/23 16:15
S44	1	(microcontroller microprocessor).ti. and @ad<="19990606" and (program$controll$2 program adj controll$2) and peripheral$1 and unit$1 and memory and external and internal and intelligent and core and clock and connection$1 and path$1 and structur$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 10:53
S45	1	(microcontroller microprocessor).ti. and @ad<="19990606" and (program$controll$2 program adj controll$2) and peripheral$1 and unit$1 and memory and external and internal and intelligent and core and clock and connection$1 and path$1 and structur$4 and hardware and unit$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 10:54
S46	0	"6598148".URPN.	USPAT	OR	OFF	2004/08/03 11:24
S47	2	("4680698" | "5379438").PN.	USPAT	OR	OFF	2004/08/03 11:24
S48	0	(microcontroller microprocessor).ti. and @ad<="19990606" and (program$controll$2 program adj controll$2) and peripheral$1 and unit$1 and memory and external and internal and DNF and nand	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 13:21

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S49	0	(microcontroller microprocessor).ti. and @ad<="19990606" and (program$controll$2 program adj controll$2) and dnf and NAND	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 13:19
S50	0	(microcontroller microprocessor).ti. and @ad<="19990606" and nand and dnf	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 13:20
S51	0	(microcontroller microprocessor).ti. and @ad<="19990606" and dnf	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 13:20
S52	413	(microcontroller microprocessor).ti. and @ad<="19990606" and nand	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 13:21
S53	7	(microcontroller microprocessor).ti. and @ad<="19990606" and (program$controll$2 program adj controll$2) and peripheral$1 and unit$1 and memory and external and internal and nand	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 13:21
S54	3	("6134707"|"6421754"|"6598148").PN.	USPAT	OR	OFF	2004/08/03 13:56
S55	23163	(microcontroller microprocessor).ti. and @ad<="19990606"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 13:58
S56	17	(microcontroller microprocessor).ti. and @ad<="19990606" and (program$controll$2 program adj controll$2) and peripheral$1 and unit$1 and memory and external and internal	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 13:59
S57	1	(microcontroller microprocessor).ti. and @ad<="19990606" and (program$controll$2 program adj controll$2) and peripheral$1 and unit$1 and memory and external and internal and intelligent and core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 13:59
S58	2	((phone wireless mpbile) and browser).ti.	USPAT	OR	OFF	2004/08/03 16:17

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S59	90	((phone wireless mpbile) and browser).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 16:18
S60	159	((phone wireless mobile) and browser).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/03 16:18
S74	119	pla$2 and GLA$2 and PLD$2 and FPGA$2 and (programmable near (logic device))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/23 16:19
S75	9	pla$2 and GLA$2 and PLD$2 and FPGA$2 and (programmable near (logic device)) and configurable	USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/23 16:20
S78	8	pla$2 and GLA$2 and PLD$2 and FPGA$2 and (programmable near (logic device)) and (configurable and interface)	USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/23 17:32
S79	13	"5870619"	USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/23 17:13
S80	3	("6598148").URPN.	USPAT	OR	OFF	2005/09/23 17:20
S84	45	(pla$2 or GLA$2 or PLD$2 or FPGA$2) and ((programmable near (logic device)) with (configurable with interface))	USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/23 17:33
S85	16	(pla$2 or GLA$2 or PLD$2 or FPGA$2) same ((programmable near (logic device)) with (configurable with interface))	USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/14 22:01
S86	1	(712/32 712/37 712/20 712/23 710/266 710/72) and (pla$2 or GLA$2 or PLD$2 or FPGA$2) same ((programmable near (logic device)) with (configurable with interface))	USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/23 19:10